High Ratio Bidirectional Hybrid Switched Inductor Converter using Wide Bandgap Transistors

Dan Hulea [1], Babak Fahimi [2], Nicolae Muntean [1], Octavian Cornea [1]
[1] Politehnica University of Timisoara [2] The University of Texas at Dallas
[1] Piata Victoriei No. 2, 300006 Timisoara, Romania
[2] 800 WEST CAMPBELL RD., EC33, ROOM 3.320, RICHARDSON, TX 75080, USA
Tel.: [1] +40-256-403-450 / [2] +1-972-883-6609
E-Mail: dan.hulea@student.upt.ro; fahimi@utdallas.edu; nicolae.muntean@upt.ro; octavian.cornea@upt.ro
URL: [1] http://www.et.upt.ro/ro [2] https://www.utdallas.edu/research/REVT

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Keywords

« Converter circuit », « Gallium Nitride (GaN) », « Efficiency », « MOSFET», «Supercapacitor».

Abstract

This paper presents a bidirectional converter (BHSI) with a hybrid structure based on a switched inductive cell which helps to achieve a higher conversion ratio. The switched inductive cell has two inductors which are connected in series and in parallel so that an additional current doubling/division is obtained. Bidirectional high ratio converters are useful in supercapacitor (SC) storage applications where the voltage of the SC has a large variation. Mathematical analysis is provided, and performances are compared to other converter topologies. Two experimental prototypes are constructed using Si-MOSFETs and GaN-FETs, and simulation and experimental results are provided in order to show the performances in terms of efficiency and stability of charge/discharge transition.

Nomenclature

t_1	first switching period	P_{Gate1}	gate drive loss of S_1
t_2	second switching period	P_{Gate2}	gate drive loss of S_2 or S_3
v_{L1}	L_1 inductor voltage	P_{Diode2}	diode conduction losses of S_2 or S_3
v_{L2}	L_2 inductor voltage	T	junction temperature
V_H	high voltage side bus	V_{T1}	voltage stress on S_1
V_L	low voltage side bus	I_{T1}	current stress on S_1
T_{sw}	switching period	t_{S1ON}	turn-on time of S_1
D	duty cycle	t_{S1OFF}	turn-off switch of S_1
f	switching frequency	Q_{G1}	total gate charge of S_1
I_{L1}	L_1 inductor current	$I_{driveON}$	turn-on gate drive current
I_{L2}	L_2 inductor current	$I_{driveOFF}$	turn-off gate drive current
I_L	current on the low voltage side	V_{DD}	gate drive voltage
I_H	current on the high voltage side	V_{SP1}	switch point voltage of S_1
Δi_{L1}	L_1 inductor current ripple	R_{ON}	total gate resistance for turn-on
Δi_{Lp}	ripple percentage of inductor current	R_{OFF}	total gate resistance for turn-off
W_{L1}	L_1 inductor current energy	R_{Gate1}	gate resistance of S_1
S	total active device stress	$R_{driverON}$	driver resistance for turn-on

η	converter efficiency	$R_{driverOFF}$	driver resistance for turn-off
P_{Out}	output power	R_{gateON}	external gate resistance for turn-on
P_{Total1}	total losses of S_1	$R_{gateOFF}$	external gate resistance for turn-off
P_{Total2}	total losses of S_2 or S_3	R_{T1}	drain-source on resistance of S_1
$P_{Switch1}$	switching losses of S_1	Q_{rr2}	reverse recovery charge of S_2 diode
$P_{Switch2}$	switching losses of S_2 or S_3	Q_{rr2_meas}	reverse recovery charge at I_{T2_meas}
P_{Cond1}	conduction losses of S_1	I_{T2_meas}	current for measuring Q_{rr2_meas}
P_{Cond2}	conduction losses of S_2 or S_3	C_{OSS1}	output capacitance of S_1
P_{Qrr1}	reverse recovery losses in S_1	R_{th}	thermal resistance
P_{Coss1}	transistor capacitance losses of S_1	T_{Amb}	ambient temperature

Introduction

High ratio converters are beneficial where one of the voltages is much higher than the other, such as supercapacitor storage applications [1], CPU supply [2], [3], telecom applications [4][5], etc. Bidirectional converters are especially useful in storage applications[1],[6], [7], uninterrupted power supplies, electric vehicles, where energy has to flow to/from the storage unit, or as an interface between various voltage busses in a smart grid [8]. The so-called hybrid converters make use of capacitive or inductive switching cells [9], so that they can achieve higher conversion ratios, and lower the stress on the switching devices. Furthermore, wide-bandgap devices can be used for a higher efficiency and faster switching frequencies to allow the use of smaller passive components [10], [11], and because of their smaller parasitic capacitance, oscillations that might appear in this topology will require a smaller damping circuit [12].

The topology presented in this paper is based on the buck converter using a switching inductive cell [9], and a boost converter accompanied by the same cell [12],[13], or from a similar bidirectional converter with coupled inductors [14], but without the need of coupling between the inductors.

Converter topology and analytical descriptions

The converter topology, from Fig. 1, is similar to the conventional buck converter with an additional inductor at the output. The two inductors are theoretically identical, which is an important aspect for this topology. The BHSI converter achieves its higher conversion ratio by using the switching inductive cell composed of the inductors L_1, L_2 and the transistors S_2 and S_3. One driving signal is used for S_1 and then is inverted to drive S_2 and S_3.

As it can be seen in Fig. 2, the two inductors are connected in series during t_1 period (i.e. S_1 – ON; S_2, S_3 - OFF) and in parallel during t_2 period (i.e. S_1 – OFF; S_2, S_3 - ON). Therefore, the current from the low voltage output (I_L) is doubled during that time. For positive inductor currents (I_{L1} and $I_{L2} > 0$), the converter works as a step-down converter, supplying current to the low voltage output (V_L); for negative currents, the converter works as a step-up converter, supplying current to the high voltage output (V_H).

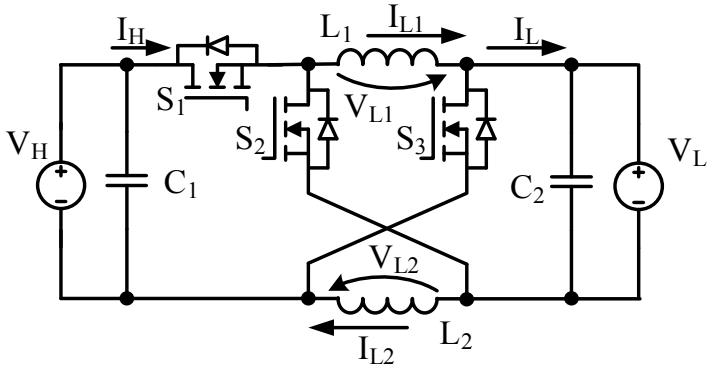

Fig. 1: BHSI schematic

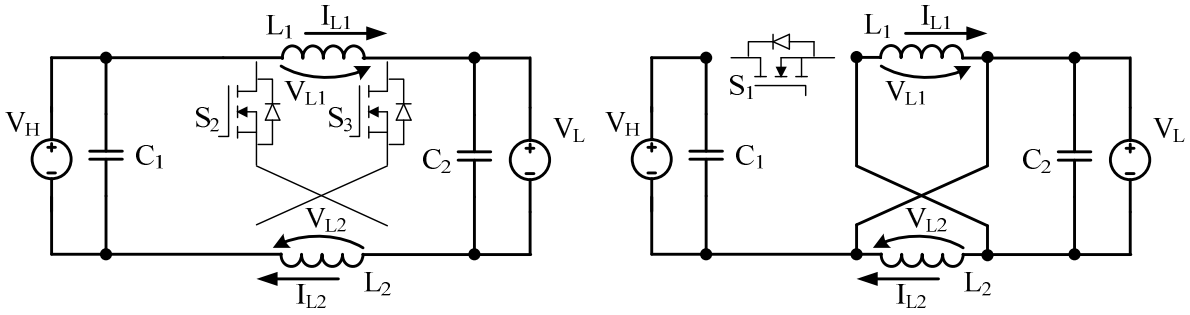

Fig. 2: BHSI during: t_1: S_1 – ON; S_2, S_3 – OFF t_2: S_1 – OFF; S_2, S_3 - ON

The main current and voltage waveforms during the two states for step down operation can be observed in Fig. 3. During t_1, the L_1 and L_2 inductor voltages are $(V_H-V_L)/2$, which is half of what a conventional converter would have been exposed to; the output and the input currents are equal to the inductor current; the S_2 and S_3 transistor voltages are equal to $(V_H+V_L)/2$. During t_2, the L_1 and L_2 inductor voltages are $-V_L$, which is equal to what a conventional converter would have; the I_L current is double of the inductor current and I_H is zero; the S_1 transistor voltage is V_H+V_L. The currents through S_1, S_2 and S_3, while they are conducting, are equal to the inductor current.

Some assumptions are made to simplify the converter analysis: the inductors are identical (therefore $I_{L1}=I_{L2}$ and $V_{L1} = V_{L2}$), the capacitors are sufficiently large to assume a constant voltage and the circuit elements are considered ideal. Taking this into consideration the equations for the inductor voltages in continuous conduction mode for the two time periods can be written as in (1).

$$\begin{cases} t_1: v_{L1} + v_{L2} = V_H - V_L \equiv v_{L1} = \frac{V_H - V_L}{2} \\ t_2: v_{L1} = v_{L2} = -V_L \end{cases} \quad (1)$$

The average inductor voltages can be written as (2), and, because in steady state the average inductor voltages will be 0, the duty ratio relation can be expressed as (3) or the conversion ratio can be expressed as (4).

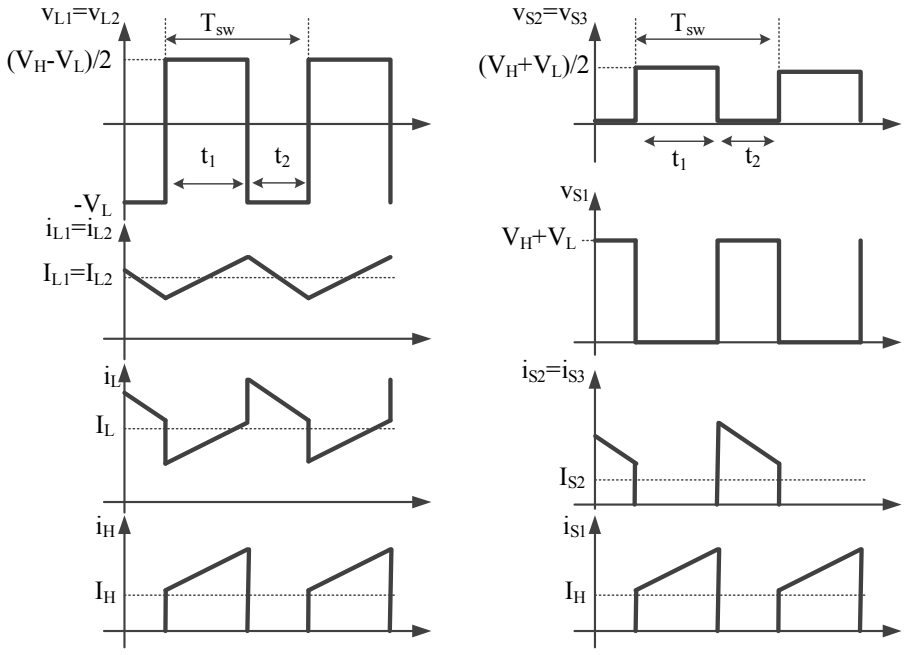

Fig. 3: Theoretical voltage and current waveforms

$$\begin{cases} \langle v_{L1} \rangle = \langle v_{L2} \rangle = D \cdot \frac{V_H - V_L}{2} + (1 - D) \cdot (-V_L) \\ D = \frac{t_1}{T_{sw}} = t_1 \cdot f \end{cases} \quad (2)$$

$$D = \frac{2 \cdot V_L}{V_L + V_H} \quad (3)$$

$$V_L = V_H \cdot \frac{D}{2 - D} \quad (4)$$

The inductor current can be expressed as a function of the output current I_L, in (5), therefore it can be observed that I_{L1} is always lower than I_L. The ripple of the inductor current, Δi_{L1}, can be considered as a percentage (Δi_{Lp}) of the inductor current, in (6), which is usually chosen to be around 10 to 15 % of the inductor current. By considering a specific percentage value for Δi_{Lp} the L_1 inductor can be calculated as in (7).

$$I_{L1} = I_L \cdot \frac{1}{2 - D} = \frac{V_L + V_H}{2 \cdot V_H} \cdot I_L \quad (5)$$

$$\Delta i_{L1} = \Delta i_{Lp} \cdot I_{L1} = \Delta i_{Lp} \cdot \frac{V_L + V_H}{2 \cdot V_H} \cdot I_L \quad (6)$$

$$L_1 = \frac{(V_H - V_L) \cdot \frac{2 \cdot V_L}{V_L + V_H}}{2 \cdot \Delta i_{L1} \cdot f} = \frac{(V_H - V_L) \cdot \frac{2 \cdot V_H \cdot V_L}{(V_L + V_H)^2}}{\Delta i_{Lp} \cdot f \cdot I_L} \quad (7)$$

In order to compare this converter to other bidirectional high ratio converters, the inductor energy (8), the total device stress (9) and the output currents ripples, (10) and (11), are calculated.

$$W_{L1} = \frac{(V_H - V_L) \cdot (V_H + V_L) \cdot \frac{V_L}{V_H^2}}{8 \cdot \Delta i_{L1} \cdot f} \cdot {I_0}^2 = \frac{(V_H - V_L) \cdot \frac{V_L}{V_H}}{4 \cdot \Delta i_{Lp} \cdot f} \cdot I_L \quad (8)$$

$$S = \sum_{j=1}^{4} V_j \cdot I_j = I_L \cdot \frac{(V_H + V_L)^2}{V_H} \quad (9)$$

$$\Delta i_L = I_{L1} + 3 \cdot \frac{\Delta i_{L1}}{2} = I_L \cdot \frac{V_L + V_H}{2 \cdot V_H} (1 + 1.5 \cdot \Delta i_{Lp}) \quad (10)$$

$$\Delta i_H = I_{L1} + \frac{\Delta i_{L1}}{2} = I_L \cdot \frac{V_L + V_H}{2 \cdot V_H} (1 + \Delta i_{Lp}/2) \quad (11)$$

A comparison between BHSI and another high ratio converter [15], is performed. In this comparison the conversion ratio, the total energy from inductors and the total active switch stress have been used as figures of merit. Even though the conversion ratio is not as good for the BHSI (Fig. 4 – left), the required inductor energy is always lower. Considering a value for the high voltage bus, V_H= 400V, and a value for the SC voltage, V_L between 20V and 100V, it can be observed that the required inductor energy for converter [15] is always higher than the BHSI ($W_{L[15]}/W_{Lbhsi}$ >1.3) (Fig. 4 – middle). The total active switch stress (Fig. 4 – right) is higher for converter [15] for V_L voltages above 35V, (which is rather small considering a 125V nominal voltage for an SC). These calculations conclude that the inductor size is smaller, and the transistors will have lower losses because of the total stress being lower, for this specific case.

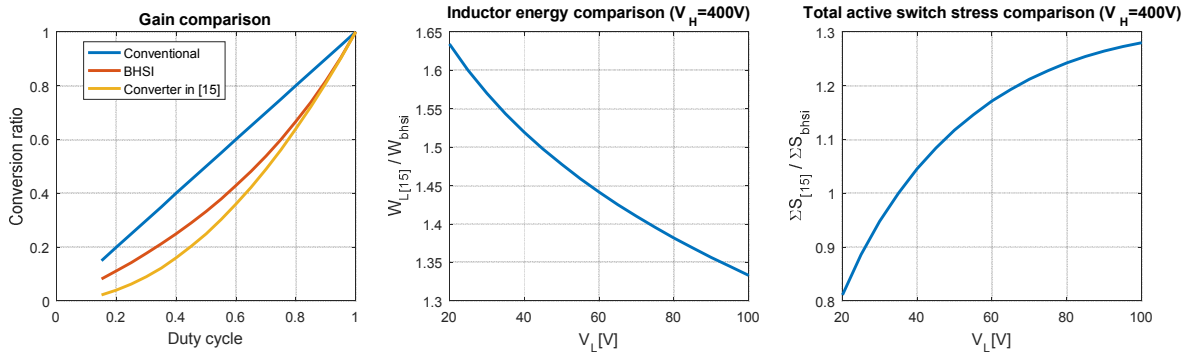

Fig. 4: Conversion ratio and inductor energy comparison for the BHSI and [15]

Efficiency calculations

The efficiency of the converter is calculated as in Appendix 1 (calculations for S_1 are shown, similar for S_2 and S_3), considering the output power the total losses from S_1 transistor and the two transistors from the switching cell, S_2 and S_3. The losses from the transistors contain the switching losses, conduction losses, reverse recovery power losses, transistor capacitance losses, and gate losses.

Two transistors have been considered for calculating the efficiency: IXFX80N60P3 for the Si MOSFETs and the TPH3207WS for the GaN FETs. The calculations were made so that the junction temperature of the transistors stay below 120°C, considering the following parameters: V_H=400V, V_L=100V, I_L changes from 0 to 50 A. The switching frequency is 80kHz using 100µH inductors for Si MOSFET and 150 kHz using 47µH inductors for GaN.

Efficiency calculations are provided for standard Si MOSFET transistors in Fig. 5 and for GaN FET transistors in Fig. 6. The graphs also show the junction temperatures, transistor power losses, and the distribution of the losses at I_L=50A as a pie chart. As expected, the GaN losses are much smaller even at higher switching frequencies.

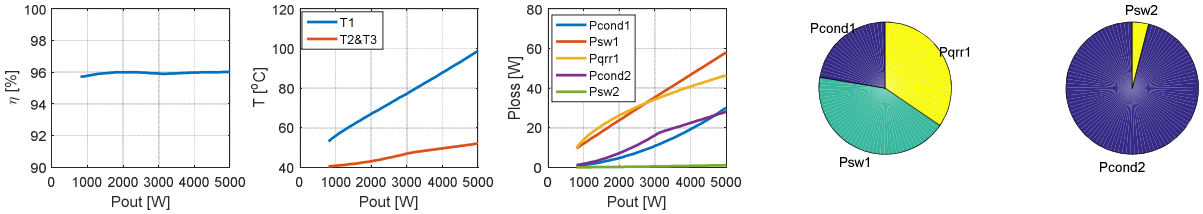

Fig. 5: Si MOSFET Efficiency calculations

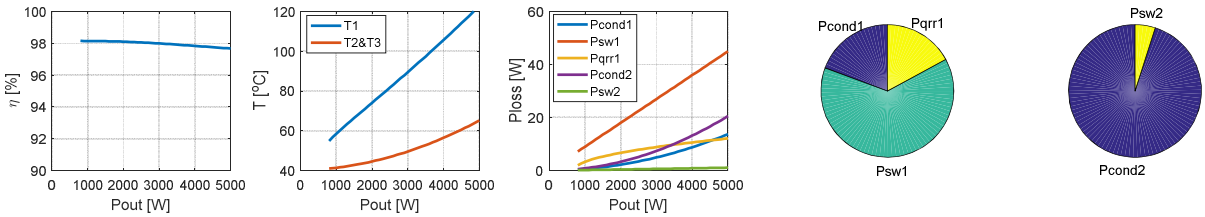

Fig. 6: GaN FET Efficiency calculations

Experimental results

Two prototypes are built using the above-mentioned Si MOSFETs and GaN devices. Multiple results have been provided to show the performances of the topology.

The initial open loop experimental waveforms of the Si MOSFET prototype (Fig. 7), show the two inductor currents and the inductor voltages, at a steady state operation. The two currents and the two voltages are almost identical, and voltage oscillations (as in [12]) are almost inexistent after using an RC snubber on one of the two inductors (R=231 Ω, C=4.7nF). The parameters for this experiment were: V_H=350V, D=40%, V_L=75.7V, I_H=3.45A, L=100µH, f=80kHz, Rload≈ 6Ω.

To test the stability of the converter while it changes its operating mode from buck to boost and vice versa, the setup from Fig. 8 was assembled. The low voltage bus (V_L) is connected to a supercapacitor of 63F with an absolute maximum rating of 125V. On the higher voltage side (V_H) a DC voltage source was connected in parallel to a constant voltage load. Both were set at a constant voltage of 300V. The DC voltage source has a diode connected at the output to protect it from reverse currents. The bus capacitor helps to stabilize the load and the source (Cbus = 10mF).

Experiments from Fig. 9 to Fig. 12 were done by implementing a current control for I_{L1} current, and having the following parameters: V_H=300V, V_L=40/60V, L=100 µH and f=40kHz. All results are compared with simulation results in order to confirm the experimental results. Step reference for the inductor current are applied as follows: Fig. 9 a step transition from -20A to 20A (left) and 10 to -10A (right); Fig. 11 a step transition from 10A to -5A (left) and -10 to 5A (right). Fig. 10 shows a close-up on a transient response (left), and a steady state response (right). As it can be seen from the waveforms, the converter has a fast response with little overshoot, and the two prototypes operate in a similar manner. In about 0.1ms (a few switching periods) the converter transitions from buck mode to boost mode and vice-versa.

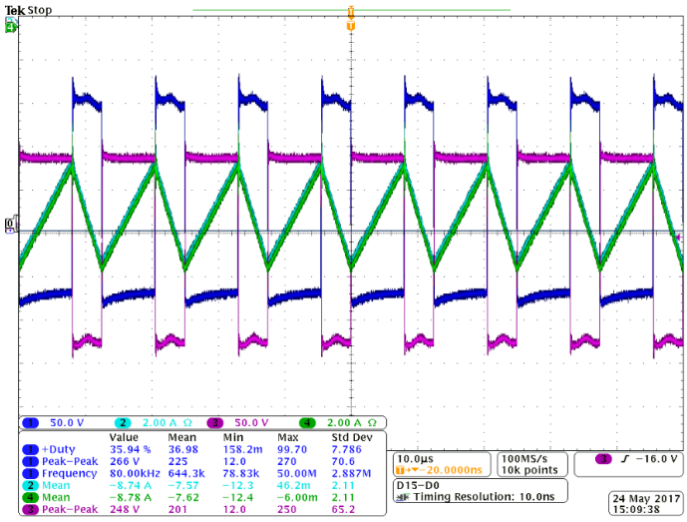

Fig. 7: (Si MOSFET) Experimental waveforms (Buck mode): **(1) V_{L1}; (2) -I_{L1}; (3) -V_{L2}; (4) -I_{L2}**

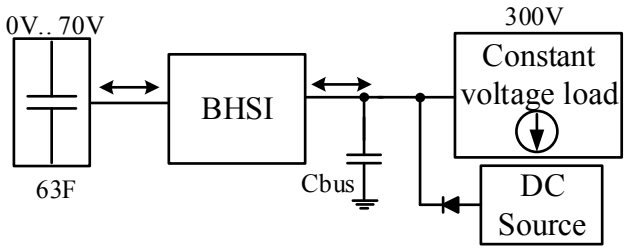

Fig. 8: Connection diagram for the test setup

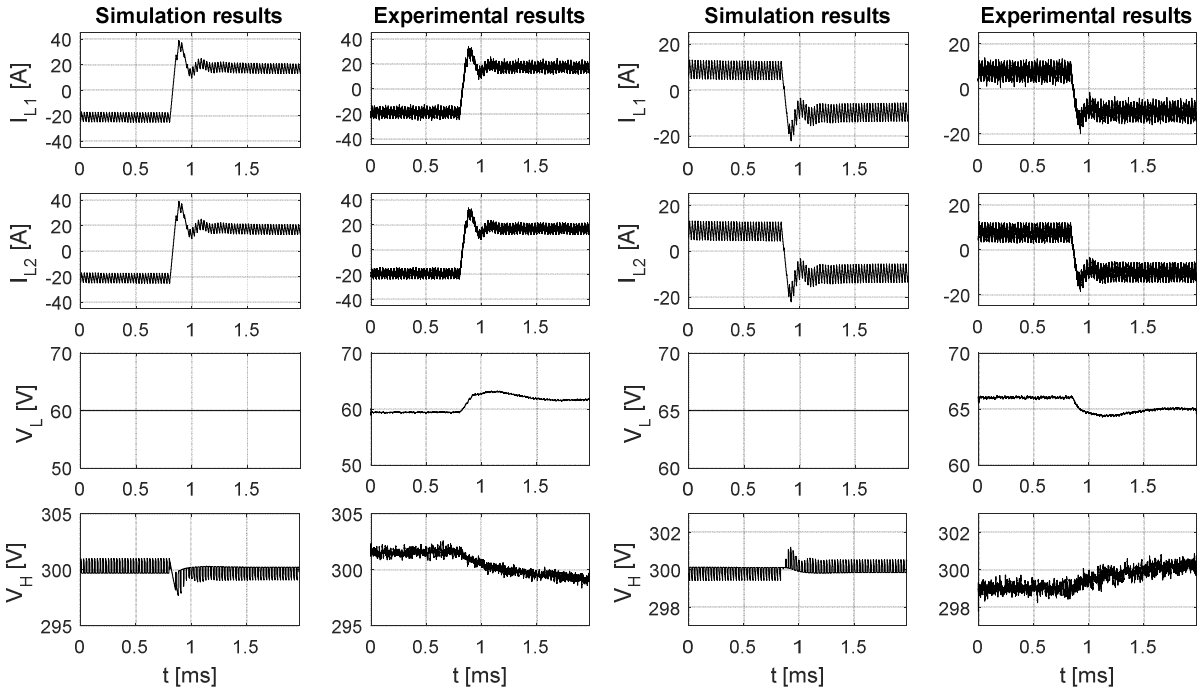

Fig. 9: (GaN)Transition between: buck/boost - left (-20A to 20A); boost/buck - right (10A to -10A);

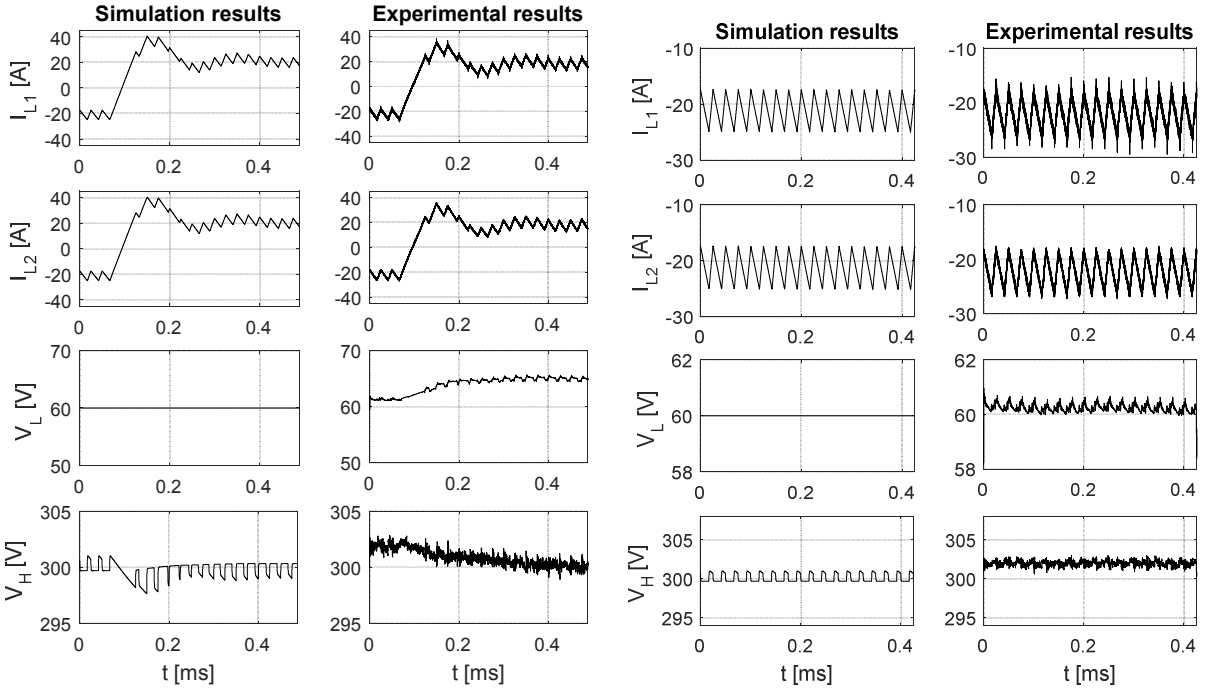

Fig. 10: (GaN) Left: Close-up on Fig. 9-left; Right: Steady state results for $I_{L1,2}\approx$-20A

The only big difference for the two prototypes is in the efficiency. Fig. 12 shows the measured efficiency for the two prototypes, compared with the theoretical values calculated as stated above. The Si MOSFET prototype has a much lower efficiency especially for boost mode, probably because of shoot-through losses on S_1. The efficiency measurements were done at the two voltages, V_L=60V and V_H=300V. The GaN prototype has efficiencies above 95%, closer to the theoretical values.
Photos of the two prototypes are shown in Fig. 13. The layout of the two prototypes is very similar, as the GaN devices come in a similar case to the Si MOSFETS.

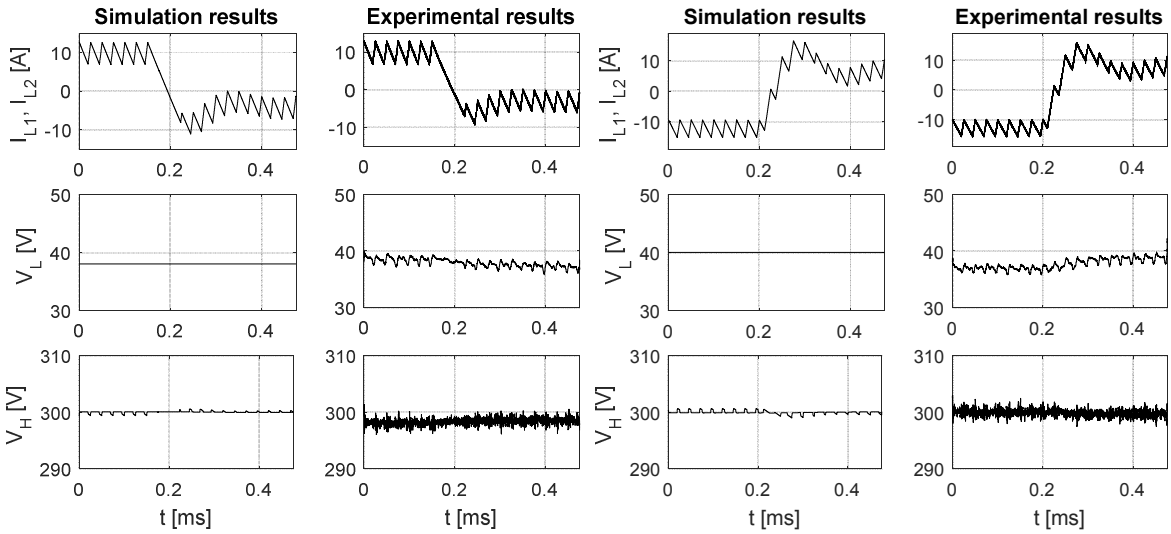

Fig. 11: (Si MOSFET) Transition between: boost/buck-left (10A to -5A); buck/boost-right (-10A to 5A);

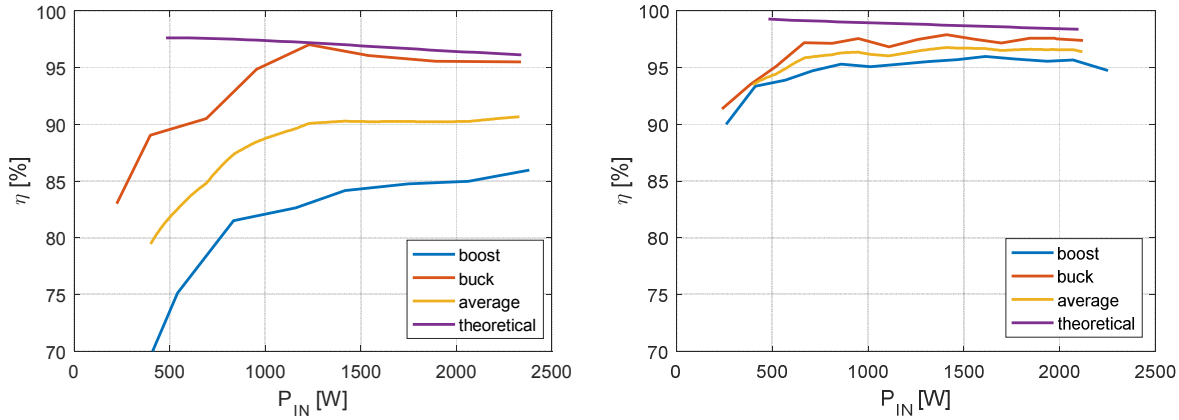

Fig. 12: Converter efficiency (V_L=60V; V_H=300V): left – Si MOSFET; right – GaN

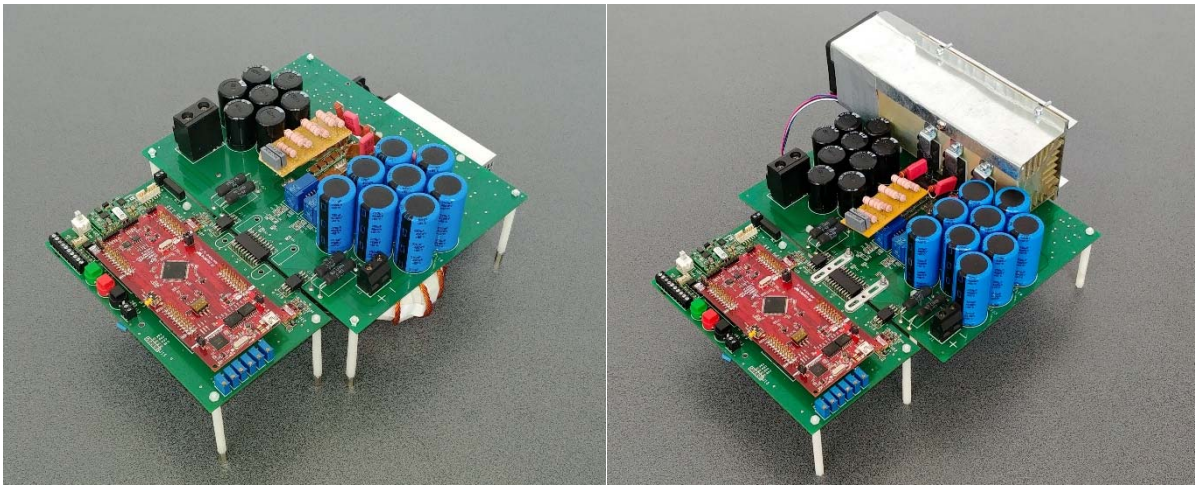

Fig. 13: Prototype photo: GaN – left; Si MOSFET – right

Conclusions

This paper analyzes a high ratio bidirectional hybrid converter by analytical and experimental means, in terms of efficiency, passive and active parts sizes. Two prototypes using Si MOSFETs and GaN FETs were tested, and the influence and benefits of the switching elements were analyzed for this configuration.
Our analysis indicates that the proposed configuration offers higher efficiency and a smaller footprint. The stability analysis and the dynamic transition between the two operating modes was also addressed showing no instability around various operating points.

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Appendix 1

$$\eta = \frac{P_{Out}}{P_{Out}+P_{Total1}+2\cdot P_{Total2}}$$

$$P_{Total1} = P_{Switch1} + P_{Cond1} + P_{Qrr1} + P_{Coss1} + P_{Gate1}$$

$$P_{Total2} = P_{Switch2} + P_{Cond2} + P_{Gate2} + P_{Diode2}$$

$$P_{Switch1} = \frac{V_{T1}\cdot I_{T1}}{2}\cdot (t_{S1ON} + t_{S1OFF})\cdot f$$

$$\begin{cases} t_{S1ON} = \frac{Q_{G1}}{I_{driveON}}; & t_{S1OFF} = \frac{Q_{G1}}{I_{driveOFF}} \\ I_{driveON} = \frac{V_{DD}-V_{SP1}}{R_{ON}}; & I_{driveOFF} = \frac{V_{SP1}}{R_{OFF}} \\ R_{ON} = R_{Gate1} + R_{driverON} + R_{GateON}; & R_{OFF} = R_{Gate1} + R_{driverOFF} + R_{GateOFF} \end{cases}$$

$$Q_{G1} = Q_{GD1} + \frac{Q_{GS1}}{2}$$

$$P_{Cond1} = {I_{T1}}^2 \cdot R_{T1} \cdot D$$

$$P_{Qrr1} = Q_{rr2} \cdot V_{T1} \cdot f$$

$$Q_{rr2} = Q_{rr2\_meas} \cdot \frac{\sqrt{I_{T2}-\frac{\Delta I_{L1}}{2}}}{\sqrt{I_{T2\_meas}}}$$

$$P_{Coss1} = \frac{C_{OSS1}\cdot {V_{T1}}^2 \cdot f}{2}$$

$$P_{Gate1} = Q_{G1} \cdot V_{DD} \cdot f$$

$$T = R_{th} * P_{Total} + T_{Amb}$$